Integral University, Lucknow

Effective from Session:							
Course Code	EC506	**Title of the Course**	VLSI Design	**L**	**T**	**P**	**C**
Year	I	**Semester**	II	**3**	**1**	**0**	**4**
Pre-Requisite		**Co-requisite**					
Course Objectives	• To understand the concepts of design of MOS/CMOS circuits and systems. • To Evaluate Low Power Design and Layout design rules and stick diagram. • To analyze basic building blocks in advance CMOS logic design, Domino CMOS logic, NORA CMOS logic, Single Phase Dynamic logic, Differential CMOS. • To understand Synchronous and Asynchronous Systems, CMOS flip flop design, Mely and Moore Machines, FSM design PSPICE simulation Programme to simulate the CMOS designs. • To identify the technology for bipolar and BiCMOS logic Gate and Gallium Arsenide Digital Circuits. • To understand and to identify the PLA, PAL, FPGA and Verilog HDL.						

Course Outcomes	
CO1	Given a system Students shall be able to understand design of MOS/CMOS circuits and systems. Able to Evaluate Low Power Design and design Layout design rules and stick diagram.
CO2	For a given system, student shall be able to analyze basic building blocks in advance CMOS logic design, Domino CMOS logic, NORA CMOS logic, Single Phase Dynamic logic, Differential CMOS, can design of Adders/Subtractor and Multiplexers/Decoder/Encoder/Multiplier.
CO3	For a given Sequential Circuit system students can understand Synchronous and Asynchronous Systems, CMOS flip flop design, Mely and Moore Machines, FSM design PSPICE simulation Programme to simulate the CMOS designs.
CO4	Students shall be able to identify the technology for bipolar and BiCMOS logic Gate and Gallium Arsenide Digital Circuits.
CO5	Students shall be able to identify the PLDs, FPGA and Implementation using Hardware Descriptive Language.

Unit No.	Title of the Unit	Content of Unit	Contact Hrs.	Mapped CO
1	Traditional CMOS Design	System approach to VLSI design. Pseudo NMOS logic, Transistor equivalency, CMOS logic and Gate design, Transmission Gate logic design, Delay of MOS circuits, Basics of Low Power Design, Layout design rules and stick diagram.	8	1
2	Advance CMOS Logic Design	Domino CMOS logic, NORA CMOS logic, Single Phase Dynamic logic, Differential CMOS, Dynamic Differential Logic, Design of Adders/Subtractor and Multiplexers/Decoder/Encoder/Multiplier.	8	2
3	Sequential Circuit Design	Synchronous and Asynchronous Systems, CMOS clock Latches, D, SR, JK, T Flip Flops, CMOS flip flop design, Synchronous design Techniques, Mely and Moore Machines, FSM design, Design of MOS SRAM, DRAM, CMOS PROMs, EPROMs, EEPROMs and Flash Memories.	8	3
4	Bipolar and BiCMOS logic Gate & Gallium Arsenide Digital Circuits	Emitter coupled logic gate, Current mode logic, BiCMOS logic gate, Alternatives BiCMOS approaches and circuits. MESFET second order effects, Logic design with MESFET, Capacitively enhanced logic and Heterojunction Bipolar Technology.	8	4
5	Design of Programmable Modules	Standard cells, PLA, PAL, PLDs, FPGA, Fused based FPGA, Mixed Analog/Digital System design, Implementation using Verilog HDL/VHDL.	8	5

Reference Books:
• Jan. M. Rabaey, Anitha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits", PHI, Second Edition
• Neil H.E Weste, Kamran Eshraghian, "Principles of CMOS VLSI Design", 2nd Edition, Pearson, 1998.
• Ken Martin, "Digital Integrated Circuits Design, Oxford Indian Edition.
• Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital IC- Analysis and Design", 3rd Edition, TMH.
• Douglas A Pucknell, Kamaran Eshragian, "Basic VLSI Design, 3rd edition, PHI, 1994.
• Wayne Wolf, "Modern VLSI Design, 2nd Edition, Prentice Hall 1998.
e-Learning Source:

	Course Articulation Matrix: (Mapping of COs with POs and PSOs)															
PO-PSO CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
CO1	3	3	3	1		1			1			2	3	2		1
CO2	3	3	3	1		1	1		1			1	3		1	
CO3	3	2	3	2	1	1			2			1	3		1	
CO4	3	3	2	2	1				1			2	3	2		
CO5	3	3	2	1					1			2	3		1	

1- Low Correlation; 2- Moderate Correlation; 3- Substantial Correlation

Name & Sign of Program Coordinator	**Sign & Seal of HoD**

Integral University, Lucknow

Effective from Session:							
Course Code	EC507	**Title of the Course**	Analog MOS Circuits	**L**	**T**	**P**	**C**
Year	**I**	**Semester**	II	**3**	**1**	**0**	**4**
Pre-Requisite	VLSI Design	**Co-requisite**					
Course Objectives	• To learn about differential amplifier and single stage MOS amplifiers. • To understand different types of MOS current mirrors and frequency response. • To tell the concept of feedback in MOS circuits and noise. • To teach about oscillators and PLL. • To impart knowledge of operational amplifiers and switched capacitor circuits.						

Course Outcomes	
CO1	Students will know about different topologies of single stage MOS amplifiers. Students will able to understand the concept of differential amplifiers.
CO2	Student shall be able to learn and understand about MOS current mirrors and frequency response of circuits.
CO3	Students shall able to know about noise in MOS circuits. Students will also learn about feedback and their different topologies.
CO4	Student will know about different oscillator circuits their operation. Students willlearn about phase lock loop
CO5	Student shall be able to know about operational amplifier and their property. Students will learn about switched capacitor circuits and their applications as amplifiers, filters, integrators and ADC/DAC.

Unit No.	Title of the Unit	Content of Unit	Contact Hrs.	Mapped CO
1	**Single Stage MOS Amplifiers**	Common source stage with resistive load, Diode connected load and Source degeneration, Source follower, Common gate stage, Cascode stage **Differential Amplifiers:** Quantitative and qualitative analysis of basic differential amplifier, Common mode response, Differential pair withMOS Loads	8	1
2	**MOS Current Mirrors**	Basic current mirrors, Cascode current mirrors,Active current mirrors **Frequency Response of Amplifiers:** Miller effect, Poles and zeroes, Analysis of CS, CD, CG stage, Cascode stage and Differential pair	8	2
3	**Noise**	Statistical Characteristics of Noise, Thermal noise, Flicker noise, Representation of noise in circuits, Noise in CS, CD, CG stage, Cascode stage and Differential pair **Feedback:** Properties of Feedback, Feedback topologies, Effect of loading in Feedback, Effect of feedback on noise	8	3
4	**Oscillators**	Oscillation criterion, Ring Oscillators, LC oscillators, Voltage controlled oscillators **Phase-Locked Loop:** Simple PLL, Charge-Pump PLL, Delay locked loop	8	4
5	**Operational Amplifiers**	Performance parameters, One stage and two stage Op-Amps, Gain boosting, Common mode feedback, Slew rate, Power supply rejection, Noise in Op-Amp, Stability and Frequency compensation in Op-Amp **Switched Capacitor Circuits:** MOS as a switch, Different switched capacitors circuits, Applications as Amplifiers, Filters, Integrators and ADC/DAC	8	5

Reference Books:

1. Razavi Behzad ”Design of analog CMOS Integrated Circuits” Tata McGraw-Hill Edition, 2002

e-Learning Source:

	Course Articulation Matrix: (Mapping of COs with POs and PSOs)																	
PO-PSO CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO4	PSO5	PSO6	PSO7
CO1	**3**	**3**	**3**	**2**	**2**	**1**		**1**	**2**			**1**	3	2	2			
CO2	**3**	**3**	**3**	**3**	**3**	**1**			**1**			**1**	3		2			
CO3	**3**	**3**	**3**	**3**	**2**	**2**			**2**			**1**		2	1			
CO4	**3**	**3**	**3**	**3**	**2**	**1**			**1**			**1**		3	1			
CO5	**3**	**2**	**3**	**2**	**2**	**2**			**2**			**1**	3	2	1			

1- Low Correlation; 2- Moderate Correlation; 3- Substantial Correlation

Name & Sign of Program Coordinator	**Sign & Seal of HoD**

Integral University, Lucknow

Effective from Session:							
Course Code	EC508	**Title of the Course**	ASIC Design and FPGA	**L**	**T**	**P**	**C**
Year	I	**Semester**	II	**3**	**1**	**0**	**4**
Pre-Requisite		**Co-requisite**					
Course Objectives	• To understand design issue in system development process. Able to perform Logical operation, Arithmetic Operation in Assembly language programming. • To analyze basic libraries in ASIC, can process CMOS and its design rule. • To understand ASIC library design, CMOS flip flop design, Library Architecture, Gate Array Design, Standard cell design Programmable ASIC Design. • To identify low level design entry, schematic entry and can understand overview of Hardware description Languages (VHDL & Verilog). • To analyze basic concept of FPGA based system, FPGA architecture, Static RAM based FPGA, Permanently Programmed FPGAs and can understand Chips I/O Circuit based design of FPGA fabrics, Architecture of FPGA fabrics.						

Course Outcomes	
CO1	Given a system Students shall be able to understand design issue in system development process. Able to perform Logical operation, Arithmetic Operation in Assembly language programming.
CO2	For a given system, student shall be able to analyze basic libraries in ASIC, can process CMOS and its design rule.
CO3	For a given transistors and resistors students can understand ASIC library design, CMOS flip flop design, Library Architecture, Gate Array Design, Standard cell design Programmable ASIC Design.
CO4	Students shall be able to identify low level design entry, schematic entry and can understand overview of Hardware description Languages (VHDL & Verilog).
CO5	For a given system, student shall be able to analyze basic concept of FPGA based system, FPGA architecture, Static RAM based FPGA, Permanently Programmed FPGAs and can understand Chips I/O Circuit based design of FPGA fabrics, Architecture of FPGA fabrics.

Unit No.	Title of the Unit	Content of Unit	Contact Hrs.	Mapped CO
1	Embedded System & Microcontroller	Introduction to Embedded System, Design issue in system development Process, Design cycle in the development phase 8051µc: Architecture, basic Assembly language programming concepts, Instruction sets, Addressing Modes, Logical operation, Arithmetic Operation, Subrouters, Interrupt handling timing subrouters, Serial Data Transmission, Serial data communication	8	1
2	Introduction to ASIC	Types of ASIC, ASICs cell libraries CMOS logic: CMOS process, CMOS designrule, combinational logic cell, sequential logic cell, Data path logic cell, I/O cells cell compilers	8	2
3	ASIC Library Design	Transistors and resistors, transistors parasite capacitance, logical Effort, library cell Design, Library Architecture, Gate Array Design, Standard cell design Programmable ASIC Design: Anti fuse, Static RAM, EPROM and EEPROM Technology	8	3
4	HDL & ASIC	Low level design Entry, Schematic Entry, low level design, language, PLA tools, EDIF, Overview Hardware description Languages (VHDL & Verilog), Logical Synthesis VHDL Simulation, ASIC Construction, Floor Planning and Placement Routing.	8	4
5	FPGA Based System	Basic Concept, Digital Design & FPGA. FPGA Fabrics: FPGA architecture, Static RAM based FPGA, Permanently Programmed FPGAs,	8	5

		Chips I/O Circuit Design of FPGA fabrics, Architecture of FPGA fabrics, Logic implementation of FPGAs Architecture		

Reference Books:

- M.J. S. Smith /Application Specific Integrated Circuits/ Pearson Edu., 2005.
- K.J. Ayla /The 8051 Microcontroller/ Paperback 3rd Edition, July 2004.

e-Learning Source:

	Course Articulation Matrix: (Mapping of COs with POs and PSOs)															
PO-PSO CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
CO1	3	2	2	1	1	1	1		1	3	2	1	3	1	1	1
CO2	3	3	1			1	1			1			3	1	1	1
CO3	3	2	2	2	1	1	1	1	1		2		3	2	1	
CO4	3	3	3	3	2	2	2		2		1		2	1	2	
CO5	3	3	2	2	3	2	1			3			2	1	2	1

1- Low Correlation; 2- Moderate Correlation; 3- Substantial Correlation

Name & Sign of Program Coordinator	**Sign & Seal of HoD**

Integral University, Lucknow

Effective from Session:							
Course Code	EC 509	**Title of the Course**	Fault modelling and testö	**L**	**T**	**P**	**C**
Year	**2nd**	**Semester**	IV	**3**	**1**		**4**
Pre-Requisite	VLSI Design	**Co-requisite**	IC Technology				
Course Objectives							

Course Outcomes	
CO1	**To Understand** the silicon crystal structures**. Identify** the orientations and explain theireffects and also nature and effects of impurities. To **apply** the Parametric problems to circuit sensitivities.
CO2	**Analyze** the Yield and failure models. **Explain** the Gate level testing and their fault models. chip level testing and their fault models.
CO3	**Design** and **analyze** of five valued logics **Describe** the application of truth table generation of standard gates, Boolean algebra its use in testing. Also to **describe** the Stuck-at faults.
CO4	**List** and **explain** the different CMOS test methods. **TO understand** Functionality and manufacturing test principles, ATPG, Fault grading, delay fault testing, Statical fault analysis designstrategies.
CO5	**To understand** the concept of Functional testing, Ad-hoc scan-based testing, self-testing. **Differentiate** between Chip level & system level testing examples.

Unit No.	Title of the Unit	Content of Unit	Contact Hrs.	Mapped CO
1	**Crystal fundamentals**	Fundamentals of silicon crystal structures, orientation planes and their effects, nature and effects of impurities like carbon, oxygen etc., Parametric problems andeffects in fabrication, circuit sensitivities	8	CO1
2	**Fault and modelling**	Yield, Yield loss, failure and models of failure analysis, Gate level testing andtheir fault models, chip level testing and their fault models	8	CO2
3	**Fault analysis**	Introduction to five valued logic, truth table generation of standard gates, Boolean algebra, its use and testing, Stuck-at faults.	8	CO3
4	**Test pattern and strategies**	CMOS test methods, Functionality and manufacturing test principles, ATPG, Fault grading, delay fault testing, Statical fault analysis design strategies	8	CO4
5	**Testing methodologies**	Functional testing, Ad-hoc scan-based testing, self-testing and IDDQ Testing,Chip level & system level testing examples	8	CO58

Reference Books:

1. Lala P.K."Fault Tolerant and Fault Testable Hardware Design" BS Publication
2. Sze S.M. "VLSI Technology" TMH Publication
3. Weste Neil H.E., Eshraghian Kamran "Principle of CMOS VLSI Design" 2nd ed Pearson
4. Hurst Stanley Leonard "VLSI Testing" IEEE Circuits and Devices Series

e-Learning Source:

	Course Articulation Matrix: (Mapping of COs with POs and PSOs)																	
PO-PSO CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO4	PSO5	PSO6	PSO7
CO1	3	3	2	1	1	1		1	1			3	2	3	2	1		
CO2	3	3	3	3	3	1			1			1	3	3	2			1
CO3	3	3	2	3	3	1			1			1	3	3	1		1	1
CO4	3	3	3	2	2				1			1	3	2	2		2	2
CO5	3	3	2	3	3				2			1	3	2	2		2	2

1- Low Correlation; 2- Moderate Correlation; 3- Substantial Correlation

Name & Sign of Program Coordinator	**Sign & Seal of HoD**

Integral University, Lucknow

Effective from Session: 2022-23							
Course Code	EC510	**Title of the Course**	VLSI Design lab	**L**	**T**	**P**	**C**
Year	**I**	**Semester**	II	**0**	**0**	**2**	**1**
Pre-Requisite	EC510	**Co-requisite**					
Course Objectives	To practice the fundamental programming methodologies using the Xilinx simulation Software for simulatingthe Combinational and sequential logic circuits. This course provides the design of various digital circuits using different VLSI simulation software tools like Modelsim and Xilinx. The outcome of this course is to learn VHDL and Verilog language and also learn the usage of different tools.						

Course Outcomes	
CO1	Acquire knowledge about High Speed VLSI Circuits Design.
CO2	. Identify the basic Back-End-Of -Line Variability Considerations.
CO3	Understand the Method of Logical Effort.
CO4	Understand the Circuit Design Margining and Latching Strategies
CO5	Understand the Clocking Styles.

Experiment No.	**Title of the Experiment**	**Content of Unit**	**Contact Hrs.**	**Mapped CO**
1	Digital basic gates	Design of basic Gates: AND, OR, NOT.	2	CO1
2	Universal gates	Design of universal gates.	2	CO1
3	2to 4 Decoder	Design of 2 to 4Decoder.	2	CO2
4	Half-Adder, Full-Adder	Design of Half-Adder, Full Adder.	2	CO2
5	Half-subtractor,Full-Subtractor	Design of Half Sub tractor, Full Sub tractor.	2	CO3
6	3:8 Decoder	Design of 3:8Decoder.	2	CO3
7	S-R Flip-Flops	Design of S-R Flip-Flops using(if-then-else) Sequential Constructs.	2	CO4
8	J-K Flip-Flops	Design of J-K Flip-Flops using(if-then-else) Sequential Constructs.	2	CO5

e-Learning Source:

https://www.vlab.co.in/

	Course Articulation Matrix: (Mapping of COs with POs and PSOs)														
PO-PSO CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	3	1	3	1	1	1	1		2	1	3	3	2
CO2	3	3	3	2	2	1			1		2	1	2	2	
CO3	3	3	3	2	2	1			1		2	1	2	2	
CO4	3	3	3	2	1				1			1	2	2	
CO5	3	3	2	2	1				1			1	2	2	

1- Low Correlation; 2- Moderate Correlation; 3- Substantial Correlation

Name & Sign of Program Coordinator	**Sign & Seal of HoD**